REVIEW

Nanopillar junctions

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The fabrication of nanopillar devices has been essential to the understanding and development of metallic spin electronics. This paper discusses the processes that can be used for the fabrication of such structures and the challenges in which they present, with particular emphasis on extreme sub-micrometre pillar structures suitable for the study of spin-transfer torque effects.

Keywords: giant magnetoresistance; spin-transfer torque switching; spintronics; magnetic random access memory; Josephson junctions

1. Introduction

The rapid evolution of spintronics was initiated by the discovery of giant magnetoresistance (GMR) in metallic multilayers by Fert and Grünberg [1,2]. GMR, the subsequently developed tunnel magnetoresistance (TMR) [3] and spin transistors of various types rely on the differential scattering or transmission of carriers with opposite spin. The simplest understanding of GMR is in a one-dimensional approximation with the current flow perpendicular to the plane (CPP) of the multilayer. However, in practical terms, this is the most difficult geometry to realize and, until the development of efficient nanofabrication techniques, the low resistance of metallic multilayers dictated that the vast majority of measurements were made with the current in plane (CIP), while CPP measurements required the incorporation of superconducting quantum interference device (SQUID) amplifiers, which necessitated low-temperature measurements.

The progressive replacement of CIP spin valves with CPP TMR junctions in hard disk read-heads, and the aggressive scaling of such devices required to achieve increased bit density, rapidly progressed the industrial capability for nanopillar device fabrication, and the increasing current densities required to drive these devices enabled the experimental observation of the spin-transfer torque (STT) effects predicted by Slonczewski [4] and Berger [5]. For definitive observation of STT and its study, the competing effects of magnetic fields induced by the sample current need to be minimized. Since the latter scale with the device dimension, while absolute critical current densities are required to induce STT,
there is a scientific need to create the smallest practical devices, with a typical length scale of approximately 100 nm. If STT is to be applied, for example as a means of electrically writing data to magnetic random access memories [6] or in the domain-wall race-track memory [7], then it is essential that reliable high-throughput processes for nanopillar fabrication can be developed.

In this paper, we will review the processes that have been developed for nanopillar junction fabrication for spintronics and the important results that have been achieved. We will then discuss some of the challenges and opportunities that remain in the field and the scientific issues that may be resolved if the technical challenges can be overcome.

2. Standard patterning processes

Metallic spintronic materials, chiefly transition metal multilayers, generally cannot be effectively etched by the highly anisotropic patterning techniques that underpin much of semiconductor device processing. The techniques available for patterning such materials can be divided into templating, which includes deposition and lift-off, and physical etching processes such as ion-milling.

(a) Templating

The first approach to templated nanopillar formation relied on electrochemical growth through thick templates. Individual wires could be patterned and measured using ion-damage tracks in polycarbonate membranes (see [8]) and sequential electrodeposition of, for example, Co and Cu to create a GMR stack [9,10]. Contact to the nanowire is provided automatically from the conducting base layer deposited on the base of the membrane from which the electrochemical growth is initiated, and by continuing the deposition process until the growing wire emerges from the pore and forms a film on the opposite surface (figure 1a). Contact to a single wire can be achieved by monitoring the resistance between the two sides of the membrane during electrochemical growth [11]. Although reasonable GMR multilayers can be grown within such templates, the deposition precision is inferior to physical vapour deposition (PVD) in terms of layer thickness control and roughness. However, because of its inherent simplicity, and the small lateral sizes of the pores (as little as 10 nm), it offered the first controllable route to CPP measurements of GMR devices. More recently, the process has been developed to enable the measurement of STT in individual nanowires [12,13]. High-density ordered arrays can also be achieved using alumina templates [14].

Lift-off processing using a lithographically patterned resist mask enables PVD growth processes to be applied but it is more useful to use etched SiO₂ templates (figure 1b), which can be retained as a dielectric layer as they are robust enough to permit further patterning [15,16].

The disadvantage of a conventional lift-off approach to CPP junction fabrication is that three lithographic steps are required (base electrode, nanopillar and counterelectrode) and two exposed interfaces are created during the fabrication process. These steps thus compromise the quality of the structure and risk introducing additional scattering at the interfaces, and so, although nanopillar structures can be fabricated by lift-off, it is more usual to prepare point-contact-type devices in which at least one of the active magnetic layers is
unpatterned [17] (figure 1c). This layer can then form part of the base connection to the structure and can assist in phase locking between arrays of STT nanopillars for microwave emission application.

A variant of conventional lift-off has been developed in which the resist mask is retained to form an isolation layer for the completed device; this has the advantage of reducing the number of process steps and exposed interfaces.

(b) Etch-back patterning

The opposite approach to templating involves deposition and etch-back. In this case, the desired film structure is deposited without prepatterning and pillars or mesas are then patterned by lithographically defined etching. Although there are potential problems in applying this technique to magnetic device systems, there are several significant advantages that outweigh these.
As the active magnetic layers are usually deposited as the first stage of a fabrication process, the layers are deposited on flat and unpatterned wafer surfaces. This means that there are no self-shadowing effects, which can cause variations of layer thickness at edges if lift-off or template processes are used. As importantly, the coating of large areas with homogeneous material enables the use of non-destructive characterization techniques, notably X-ray and neutron diffraction and magnetometry, prior to device fabrication. This enables the direct linking of structural and magnetic behaviour to device transport behaviour, with the caveat that patterning of nanopillars results in substantial magnetostatic fields, which are not present in the unpatterned state.

The transition metals that form typical magnetic device stacks cannot be easily removed using the selective chemical plasma etching techniques developed for semiconductors, primarily because volatile end-products do not exist [18]. As a consequence, the patterning of nanoscale features requires physical etching processes, usually Ar ion-milling, in which a film is sputtered by energetic incoming particles. Such processes offer only limited selectivity between different materials and so, in order to terminate the process at a particular level, accurate timing or end-point detection is required. Nevertheless, ion-milling can be accurately controlled in practice so that, for example, one magnetic layer can be left unpatterned to form a point-contact geometry in which magnetostatic coupling is minimized [19,20]. Ion-milling also results in redeposition of sputtered atoms, which can coat the side walls of the nanopillars and potentially modify their electrical properties by, for example, short-circuiting a tunnel barrier. Developments in plasma etching techniques may allow this process to be used for tunnel device fabrication, with the potential benefit that optical emission end-point detection and etch rate uniformity over larger areas can be used to terminate the etch exactly at the barrier level and hence minimize the risk of barrier shorts [21].

To achieve nanometre dimensions in the research laboratory, electron beam lithography (EBL) is required. Electron-sensitive resists typically have a poor resistance to ion-milling and so it is usual to pattern in the first instance by lift-off deposition of a hard mask, usually a metal such as Pt, Au or Cr, as the mask cannot be removed and electrical contact to the pillar is required [22]. Figure 1d shows a typical structure fabricated using such a process: a metal mask deposited by lift-off is used to define the ion-milling of a magnetic device stack. As ion-milling is unselective and only moderately anisotropic, this results in significant etching and tapering of the mask, which is, in turn, transferred into the overall shape of the pillar. Since the mask is not removed, it cannot be used subsequently to define an isolation layer and so a dielectric layer has to be formed by spin-coating (as in the example) or by uniform deposition followed by planarization. Finally, contact to the top of the pillar is made by a further metal deposition; the quality of the contact is obviously sensitive to the quality of the interface, which can introduce significant additional resistance and, in the case of high-current spin-torque devices, can lead to substantial localized heating.

Etch-back processing is now highly developed because of the adoption of TMR devices for hard disk read-out. This has facilitated the development of tunnelling STT devices [23] and ferromagnetic resonance diodes [24]. The level of complexity possible using commercial fabrication tools is demonstrated by the STT memory cell of Braganca et al. [25].
3. Novel patterning processes

The study of magnetic nanodevices has stimulated some imaginative approaches to overcome the problems inherent in the standard processes described above. In their current implementation, these processes are only suitable for research-scale fabrication.

(a) **Atomic force microscope templating**

The nanoscale tip of an atomic force microscope (AFM) can be used as a means of various lithographic processes (see [26,27]). Generally, however, rather delicate nanostructures are created by this process, which are unsuited for inorganic device fabrication. However, by using physical displacement of photoresist, Bouzehouane et al. [28] demonstrated a technique that has wide application. The key to the success of the process is the use of a conducting AFM tip: as this is lowered, the very thin (approx. 40 nm) insulating resist layer is displaced under the applied stress. The tip–sample resistance can be monitored and, by terminating the tip movement once contact is established, damage to the underlying device layers (which would normally have much higher elastic moduli than the resist) can be minimized but the creation of a clear via hole through to the sample is confirmed. The remaining resist then forms the dielectric isolation of the device, which places some constraints on subsequent growth temperatures and device operation frequencies (figures 1e and 2). A further constraint is the quality, in
terms of the presence of contaminants and hence increased resistance, of the small-area *ex situ* contact formed. Nevertheless, this technique has been used to make point-contact devices with a variety of materials systems: for example, contacts to tunnel barriers in oxide device systems [29]. This process has also been demonstrated as a flexible process for the contacting of individual nano-objects, which could include nanopillars within arrays [30]; here the topographic imaging mode of the AFM is used to locate the desired feature, and then the tip is used to create a contact via hole. The problem with this approach is that the via contact area is inevitably substantially smaller than the overall nanopillar area and so, for such a technique to be viable for magnetic nanopillar devices, the intrinsic resistance of the nanopillar should be substantially higher than that of the contact. This is possible if tunnel devices are to be measured, but unlikely for diffusive devices.

(b) *Focused ion beam device fabrication*

A focused ion beam (FIB) system emits a stream of ions, usually Ga, which can be scanned and blanked as in an EBL system. These ions can sputter or implant into the sample surface and so can be used as a method of direct patterning. Such systems are now relatively standard in a research environment and are an excellent prototyping route for device fabrication.

The use of FIB systems for nanopillar fabrication was pioneered by Kim *et al.* [31], who used it to create devices in Bi-based high-temperature superconductors. The aim was to pass current through a small number of unit cells in the *c*-axis direction to investigate the intrinsic Josephson junctions formed within this highly anisotropic class of superconductor. The FIB process was developed in order to overcome problems with earlier fabrication routes associated with heating at the contacts to conventionally formed mesas and the small lateral size of the pillars necessary because of the small Josephson penetration depth.

Initially, the process relied on monolithic nanocrystals and sequential milling from opposite sides of the sample—a typical process route is shown in figure 3. The structure formed enables contact to the top and the bottom of the pillar via undamaged superconductor and so it is reasonable to ascribe all residual heating effects in the devices to the resistive heating of the multiple Josephson devices.

Bell *et al.* [32] demonstrated that a variant of this process could be applied to create nanopillar devices in a wide variety of thin-film functional materials, including light-emitting diodes and artificial Josephson junctions in metallic multilayers. This process requires conventional FIB patterning to create a narrow construction in a wire containing the active heterostructure; the width of this wire determines one of the lateral dimensions of the device. Lateral cuts made by reorienting the sample by almost 90° isolate the nanopillar element and define the orthogonal lateral dimension (figure 1f). With suitable materials systems, the process can be used to fabricate pillars as small as 100 × 100 nm². Because the film multilayer structure is not constrained by the patterning process, either by resist thickness, which would limit stack thickness during lift-off, or by mask erosion, which would limit stack thickness during milling, arbitrarily large thicknesses can be processed using this technique: Leung *et al.* [33] used this process to measure the perpendicular-to-plane spin diffusion length of Cu thin films.
Figure 3. Nanopillar processing route from a monolithic single crystal (reprinted with permission from Kim et al. [31]).

(figure 4). Recently, the process has been demonstrated as an effective method of patterning nanopillar devices for studies of Josephson junctions containing various magnetic barriers [34–38] and for CPP magnetoresistance and STT studies [39–41].

The primary limitation of the process is the potential for resputtering of material onto the device side walls, a more severe problem than for conventionally ion-milled mesas because of the depth to which material needs to be removed and hence the volume of material that may be resputtered. This restricts its straightforward application to low-resistance diffusive devices; the few reports in the literature on FIB tunnel junction fabrication [42,43] note the tendency for this redeposited material to short the device and so its elimination by anodization is required [42].

A further limitation is the inevitable implantation of Ga ions in a film surface during imaging and milling. Implantation of Ga can result in a severe modification of a material’s crystal structure and electronic properties. This is a problem when creating superconducting-based devices and, in particular, devices in which the higher-temperature oxide superconductors are used owing to the sensitivity of these complex materials to impurities [44]. Nevertheless, Ga
ion implantation can be minimized by optimizing the FIB process. In fact, Ga ion implantation is another way in which device structures can be created or a material’s properties modified in a relatively controlled way; for example, an FIB system has been used to modify the interface anisotropy of magnetic multilayer systems [45,46] or the volume magnetization [47]. More constructively, Ga ion implantation has now been used to create artificial magnetic domains, which has enabled the angular dependence of magnetic domain-wall resistance to be measured [48].

(c) Self-assembly

The ordered growth of chequerboard structures in which rectangular columns of the functional device stack alternate with dielectric spacers has been realized in a number of materials systems; for example BiFeO$_3$/Sm$_2$O$_3$ [49]. This process relies on epitaxial growth-mode phase separation of the components and seems most easily induced in oxides. Zavaliche et al. [50,51] demonstrated local electrical contact to BiFeO$_3$/CoFe$_2$O$_4$ columnar nanostructures using scanning probe microscopy as a proof of principle for ultrahigh-density data-storage schemes.

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Figure 5. Possible four-terminal measurement geometries for a nanopillar. In general, passing the current between A and C (measuring voltage between B and D) will result in a different resistance measurement from A and D (measuring voltage between B and C).

4. Nanopillar devices for spintronics

(a) Current homogeneity

The essential purpose of any nanopillar structure for spintronics is to polarize a current bypassing carriers through a ferromagnetic layer and then allowing them to interact with other magnetic subsystems within the structure. The current flow can be: diffusive, as in a CPP spin valve measurement; ballistic, as in some semiconductor spintronic devices; or tunnelling through insulating layers. Except in some special cases, the devices are formed by conventional thin-film deposition processes and so the lateral dimensions, even if defined by high-resolution lithography, are often larger than the vertical thickness of the device stack. Therefore, the degree to which their behaviour can be considered one-dimensional depends greatly on the relative impedances of the active layers and the lead structures that feed them. Where the ratio of the former to the latter is large, for example, for thick tunnel barriers or where superconducting leads are incorporated, then the situation is straightforward because the layers within the nanopillar form equipotential surfaces. At the opposite extreme, current flow can be highly inhomogeneous, leading, for example, to geometric effects that can appear to enhance the magnetoresistance [52]. Figure 5 illustrates the behaviour of a homogeneous pillar device fed by crossed wires, which creates in principle a four-terminal measurement configuration. In a true four-terminal configuration, applying the current to A–C and measuring the voltage across B–D should yield the same result as applying current to A–D and measuring across B–C. For large ratios of the lateral dimension \( L \) to the vertical height \( t \), the measured resistance in the two cases will, respectively, tend to zero and \( \rho L/w \), where \( w \) is the device width (essentially a CIP measurement), and both configurations will only tend asymptotically to the correct CPP value of \( \rho t/Lw \) for \( L \ll t \).

Ozatay et al. [53] deliberately introduced a constriction within a nanopillar by EBL patterning of an Al₂O₃ layer within the stack and then performing a standard etch-back nanopillar definition aligned with this pin-hole (figure 6). As with magnetic inhomogeneity (see below), reversal and precession are assisted by domain-wall nucleation by the high localized current density. Current inhomogeneity can be induced via self-assembled ‘nanocurrent channels’ in nanocomposite materials such as FeSiO [54].

(b) Magnetostatic fields

In conventional spintronic multilayers, magnetostatic fields largely arise from roughness-induced surface poles. The ferromagnetic coupling between adjacent...
magnetic layers induced in this way is illustrated in figure 7a and is termed Néel or ‘orange-peel coupling’ [55].

As device dimensions are reduced, and the magnetic layers within stacks are more likely to become single-domain, then structural magnetostatic fields become more important. Such dipole fields scale approximately as $1/L$, where $L$ is the device dimension parallel to the moment, and so this form of coupling will tend to dominate in nanopillars as illustrated in figure 7b [22] and enforce an antiferromagnetic coupling between adjacent layers. Self-evidently, this coupling between adjacent magnetic layers can be eliminated if the materials are unpatterned but the current flow is limited by mechanical [56,57] or masked [17] point contact injection.

In STT spin valve devices, dipole fields acting on the free magnetic layer can be reduced by the incorporation of a synthetic antiferromagnet (sAF), which fixes one of the magnetic layers; however, their presence can result in a reduced STT effect on the free layer [58]. Magnetostatic fields in patterned nanopillars can be advantageously engineered to enhance STT by introducing magnetic inhomogeneity, which reduces the required switching currents of the device [59], or by stabilizing precessional modes [60].

In superconducting devices containing magnetic barriers, the flux associated with the barrier also interacts with the phase of the superconducting order parameter. In micrometre-scale junctions incorporating strong ferromagnetic barriers, this flux greatly exceeds the flux quantum $\Phi_0$, and so the critical current at zero applied field is heavily suppressed [61]. To overcome this, composite barriers in which magnetic layers are exchange-coupled to form a sAF have
been introduced [61], even though this greatly modifies the dependence of the critical current on barrier thickness [62]. For example, the recent discovery of controlled triplet superconductivity in ferromagnets (FMs) relied on sAF barriers where micrometre-scale junctions were used [63], but could be demonstrated in homogeneous FMs using nanopillar devices [64].

(c) Elimination of series resistance and non-local measurements

As discussed in §4a, unless superconducting contacts are used, currents through nanopillar devices will only approximate a CPP configuration. Consequently, thick leads and small device areas are necessary. Even where this can be achieved, the field-independent series resistance associated with leads can significantly reduce the apparent magnetoresistance. Conventionally fabricated nanopillar structures can largely eliminate this by using a four-terminal cross-geometry.

This is less straightforward with the FIB process (§3b) because of the one-dimensional nature of the nanowire initially created. However, starting with a lithographically defined cross, it has been shown to be possible to create a four-terminal Kelvin bridge device structure (figure 8) [65].

For STT devices, lateral and non-local devices have been recently demonstrated [66]. These devices enable pure spin currents to be detected using a non-local spin valve structure. To fabricate these devices, a multi-step process is required, which involves interface cleaning stages. For optimal device operation, fabrication methods in which no interface is exposed during the processing are desirable, such as the angled deposition method of Otani et al. [66].
The FIB process opens an intriguing opportunity of fabricating a vertical variant of non-local devices as shown in figure 1g. In the FIB fabrication process, all the layers are deposited in a single vacuum cycle and interfaces are cleaner than in the multi-stage lateral device fabrication. This provides better control on interface properties, which can be engineered during the growth process and are unaffected by the fabrication processes. In the vertical non-local spin valve structure, electrons are injected from the bottom FM to the spacer layer. Rather than flowing through the second FM, the charge current flows out of the spacer layer and the spin current into the top FM layer. A pure spin current can also deliver spin torque \[66\] and hence can drive the magnetization of the top layer without any charge current flowing through it. No vertical non-local spin valve device has yet been demonstrated but such a device could be ideal for studying the role of interface in spin torque being transferred through pure spin current.

(d) Magnetic dead layers

A further non-ideality factor for spintronics devices comes from the quenching of magnetism at the surface of a magnetic thin film and, in particular, at the interface of these films with other non-magnetic materials \[67–69\]. In a Josephson junction containing a Co/Ru/Co synthetic antiferromagnetic barrier, these magnetically dead layers have recently been shown to result in a significant loss in spin memory owing to enhanced spin scattering associated with these intermixed interfaces \[61\]. Such magnetically quenched interfaces are a particular issue for nanopillar devices owing to the finite scale of these systems and thus to the associated resistance of these layers to the total resistance of a device. Physically, the scale of these magnetically dead layers can correspond to a significant fraction of the total magnetic thin-film thickness. To minimize the extent of these magnetically dead layers, magnetic materials with appropriately matched band structures can be chosen; it was recently demonstrated that the magnetically dead layer at the surface of Co could be eliminated by interfacing with Rh in a Nb/Rh/Co/Rh/Nb superconducting device structure \[37\]. It was concluded that the isoelectronic nature of an Rh/Co interface means that any d–d hybridization between Co and Rh results in an effective increase in the spin–orbit splitting of the Co orbitals and thus in an increase in the orbital moment \[70\].

5. Summary and conclusions

Driven by the interest and challenges of metallic spintronics, a variety of techniques have been developed for nanopillar fabrication. These have enabled important developments, particularly in the understanding and optimization of STT effects. Very recently, we demonstrated that the high CPP current densities made possible by the nanopillar geometry enabled the observation of a non-equilibrium magnetic effect, whereby the magnetoresistance was current-density-dependent, implying that the electronic structure of the thin magnetic layer affected could be modified by spin accumulation \[40\].

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