Nanofabrication, effects and sensors based on micro-electro-mechanical systems technology

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In this paper, our investigation of nanofabrication, effects and sensors based on the traditional micro-electro-mechanical systems (MEMS) technology has been reviewed. Thanks to high selectivity in anisotropic etching and sacrificial layer processes, nanostructures such as nanobeams and nanowires have been fabricated in top-down batch process, in which beams with thickness of only 20 nm and nanowires whose width and thickness is only 20 nm were achieved. With the help of MEMS chip, the scale effect of Young’s modulus in silicon has been studied and confirmed directly in a tensile experiment using electron microscopy. Because of their high surface-to-volume ratio and small size, silicon nanowire (SiNW)-based field-effect transistors (FETs) have been shown as one of the most promising electronic devices and ultrasensitive detectors in biological applications. We demonstrated that an SiNW–FET sensor can reveal ultrahigh sensitivity for rapid and reliable detection of 0.1 fM of target DNA with high specificity. All these indicate that the MEMS technology can pave the way to nanoapplications with its advantages of batch production, low cost and high performance.

1. Introduction

In the past decades, nanotechnology has drawn a lot of attention for its novel properties in nanomaterials and dramatic behaviours in nanodevices. As nanoscaled structures behave differently from their counterparts at macro- and microscales, a lot of methods have been developed to realize nanofabrication, such as X-ray...
lithography, electron beam lithography [1–4], nanoimprint lithography [5–8], focused ion beam (FIB) nanolithography [9,10], single atom manipulation [11], quantum dot self-assembly process [12–14] and so on.

As one of the most important materials in modern semiconductor manufacture, silicon, now it can be scaled down to nanometres, has attracted much attention for its potential use not only in electronic devices but also in ultra-sensitive sensors [15–17]. However, the mass production of nanostructure silicon has suffered from the lack of suitable fabrication technologies, thus causing a great interest in finding new fabrication technologies for silicon nanostructures over the past few decades.

For example, the existing methods to fabricate silicon nanowires (SiNWs) can be generally classified as bottom-up and top-down approaches. The bottom-up approach assembles molecules and small solid structures from atoms, which have been successfully synthesized into nanostructures over the past decades [18]. However, although different strategies have been explored in integrating the synthesized nanowires into devices [19,20], there are still challenges in developing a suitable controlled alignment method.

In the meantime, structural dimensions of microelectronics and micro-electro-mechanical systems (MEMS) devices are going into submicrometre field. As a typical top-down method, its high selectivity in anisotropic etching and sacrificial layer process makes it possible to develop suitable methods controlling the production of the nanostructures more precisely.

Furthermore, MEMS can also be a good assistant to investigate nanoeffects. Being a research focused on nanoelectronics and nano-electro-mechanical systems (MEMS) devices are going into submicrometre field. As a typical top-down method, its high selectivity in anisotropic etching and sacrificial layer process makes it possible to develop suitable methods controlling the production of the nanostructures more precisely.

In this paper, we review our approach based on MEMS technologies to produce Si nanostructures, and nanoeffects, as well as high-performance nanosensors [35–50].

2. Nanofabrication based on high-selectivity micro-electro-mechanical systems processes

To our knowledge, the key point of MEMS technology is its high selectivity especially in the processes of anisotropic wet etching, sacrificial layer process and dry etching [30,51]. Anisotropic wet etching is based on the fact that different crystalline planes of silicon have different etch rates in alkaline solution, including KOH, tetramethylammonium hydroxide (TMAH), etc. [52–57]. Therefore, silicon with different planes has different etching performance, which makes silicon a good material in bulk micromachining. Sacrificial layer process is one of the most important technologies in surface machining. Generally, it has five basic steps. After the deposition and patterning of the sacrificial and structure layer as well as the removal of sacrificial layer, a three-dimensional structure can be formed. The success of this process is strongly dependent on the selectivity of etch rate in an etchant. Dry etching is another etching method to form the structure [58,59], in which the etch reactants appear in gas or vapour phase, and in most of the cases they are ionized. Compared with the wet etching process, its selectivity depends on the mask and
Figure 1. Principle and set-up of the galvanic etch stop. (a) Au, Si and TMAH form a galvanic cell. (b) $p-n$ junction galvanic etch stop.

Galvanic etch stop is very attractive for its precise control over the thickness of microstructures. The Au layer, Si and TMAH form a galvanic cell, as shown in figure 1a. When the Au : Si area ratio is larger than a threshold value, the cathodic current is large enough to cause formation of a thin layer of SiO$_2$ on the Si surface. The thin SiO$_2$ layer protects Si from TMAH etching. The threshold Au : Si area ratio was reported to be 8 : 1 [60,61]. The $p-n$ junctions are used to selectively etch Si structures, as shown in figure 1b. As the $p-n$ junctions are inversely biased, $p$-type Si layers are not protected by galvanic cells. The $p$-type Si layers are etched by TMAH and the etching stops after reaching $p-n$ junction. The drawback of the technique is that as the potentials of $p$-type Si layers are not well defined, the etching stops several micrometres before reaching the $p-n$ junction, which means that the technique cannot be used for fabrication of submicro/nanobeams.

As the cathodic current is large enough only when Au : Si area ratio is larger than the threshold value, it is possible to trigger the etch stop with the change of Au : Si area ratios before and after the release of the beam. A simple process flow has been proposed to fabricate single-crystal silicon (SCS) submicro/nanobeams on standard wafers with anisotropic wet etching and galvanic etch stop, as shown in figure 2. The structure shown in figure 2a is fabricated first in a (111) Si wafer. The submicro-/nano-thick step is shaped by a shallow dry etching and passivated with the SiO$_2$ layer. The step is perpendicular to $\langle 110 \rangle$ orientation. The depth of the step is equal to the design value of the beam thickness. The step is connected to Cr/Au wires, which serve as the Au electrode for galvanic etch stop. The area ratio between the Au electrodes and the step is larger than the threshold ratio. Then, the structure is etched by TMAH. As the submicro/nanostep is not released from the substrate yet, the exposed area of Si surface is equal to bottom surfaces of the trenches. The Au : Si area ratio is designed to be smaller than the threshold ratio. Si is etched by TMAH. After the beam is fully released from the substrate by TMAH etching, the Au wires are connected to the beam and isolated to the substrate, as shown in figure 2b. The area ratio between the Au wires and the beam is larger than the threshold ratio. The galvanic etch stop is triggered and TMAH does not etch the beam anymore. After SiO$_2$ is etched away, the submicro/nanobeam supported by Au wires is fabricated, as shown in figure 2c. The length and the width of the beams are determined by photolithography. The thickness of the beams is approximately determined by the dry etching, which can be accurately controlled. The gaps between the beams and the substrates can also be determined by the dry etching. As the Au wires are designed to be much stiffer than the Si beams, the resonant frequency of the whole structure is
Figure 2. Process flow. (a) Structure before etching. (b) When the submicro/nanobeam is formed, the Au : Si area ratio is larger than the threshold ratio. The beam is protected by galvanic cell etching. (c) After SiO$_2$ is etched away, the submicro/nanobeam supported by Au wires is fabricated.

Figure 3. Submicrometre beams were fabricated in (111) wafer. (a) SEM image of a sample, the scale bar is 50 μm. (b) Close-up of the beam, the scale bar is 500 nm.

determined by the Si beam. In principle, the submicro/nanobeams can be fabricated in Si wafers with different orientations by galvanic etch stop.

Scanning electron microscopy (SEM) images of a submicrometre beam are shown in figure 3. The thickness is measured to be 530 nm. The tilting of the sample, which is 45°, is considered. Experiments showed that the beam thicknesses did not change with over etching, even if the SiO$_2$ layers on the surface of the beams were stripped.

(b) Silicon nanobeam in (111) silicon wafer [40]

Nanobeams can be made by anisotropic wet etching in standard (111) Si wafers [62–64]. However, the beams are always electrically connected to the substrate, making it difficult to use them in
Figure 4. The double-clamped nanobeam supported by Au wires. The beam is 32 μm long, 20 μm wide and 147 nm thick. The Au wires are 5 μm thick. The gap between the beam and the substrate is about 10 μm. (a) A double-clamped nanobeam supported by Au wires. (b) Close-up of the beam.

We have developed a modified process, which can fabricate single-crystal nanobeams electrically isolated from the (111)-oriented Si substrate.

The process flow is similar to that shown in figure 2, except that KOH instead of TMAH is used to etch the wafer and only (111) Si wafers can be used. The galvanic effect can be neglected in KOH solution. The thickness of the beam and the gap between the beam and the substrate are determined by the dry etching and KOH etching processes. The etch rate of (111) Si plane is about 38 nm h$^{-1}$ in 45 wt% KOH at 50°C. After the single-crystal nanobeams are fully released from the substrate by KOH etching, the thickness of the beams decreases with further KOH etching. Beams as thin as 47 nm have been obtained with the method. The length and width of the beams are determined by photolithography. The thickness of the beam and the gap between the beam and the substrate are determined by the dry etching and KOH etching processes. Double-clamped beams and cantilever beams have been fabricated.

Figure 4a shows an SEM image of a double-clamped beam structure. Figure 4b shows that the thickness of the beam was measured to be 147 nm, as the sample tilt was 80°. When the gaps between the beams and the substrate were 10 μm, more than 70% of the structures withstood the etching and the drying processes. Figure 5 shows an atomic force microscopy (AFM) picture of the surface of a beam. The r.m.s. roughness was measured to be 1.08 nm in an area of 5 × 5 μm.

(c) Silicon nanobeam on (110) silicon-on-insulator wafer [39]

We also developed a new process to fabricate nanobeams on (110) silicon-on-insulator (SOI) substrate. According to the crystal structure of silicon, its (111) crystal surface is perpendicular to the (110) surface and the intersect line of both is ⟨112⟩ crystal direction. It is feasible to define
Figure 5. AFM picture of a beam surface. The r.m.s. roughness is 1.08 nm in an area of 5 × 5 μm. (Online version in colour.)

Figure 6. (a, b) Etch process of silicon nanobeams in (110) SOI wafer.

the length direction of mask along with ⟨112⟩ direction on a (110) wafer. After anisotropic wet etching, vertical (111) sidewalls are obtained because of much slower etching rate of the (111) surface [20]. In our method, FIB is applied to modify middle zone of mask above silicon beam, as shown in figure 6a, and then silicon substrate is placed into anisotropic etching solution. (111) planes are developed first from the middle zone of silicon beam sidewalls, and spread to the two ends of the beam, which leads to etch stop in width direction, as shown in figure 6b. Using high-resolution FIB, the width of silicon beam can be controlled precisely at the nanometre scale. By above-mentioned processes, a crystal silicon nanobeam of 25 μm long, 122 nm wide and 7 μm thick is obtained, as shown in figure 7. This method features some merits such as no surface damage and good repeatability.

(d) Silicon nanowire on (100) silicon-on-insulator wafer [35,36,45]

With anisotropic wet etching and sacrificial layer process, SiNW can also be fabricated. The fabrication process can be seen in figure 8. The first oxidation and photolithography on a (100) SOI wafer is followed by a KOH or TMAH etching, which defines a step on the top silicon layer (figure 8a). Then, silicon nitride is deposited on the wafer to cover the step, and a window is
opened on the silicon nitride to expose one side of the step (figure 8b). After the silicon oxide layer is removed as shown in figure 8c, a process of KOH or TMAH etching would be self-stopped when a triangular cross section is formed with the help of Si nitride mask (figure 8d). After removing Si nitride, the nano-Si wire with two (111) surfaces will be fabricated (figure 8e). Finally, the nanowire can also be released by buffered hydrofluoric acid (BHF) solution. The critical point during the KOH etching is shown in figure 8d. In general, we will stop the etching process a little earlier, and then we can decrease the dimension of the nanowire using oxidation process.

During the fabrication process, Si$_3$N$_4$ acted as sidewall protection layer and SiO$_2$ as mask for Si (111) planes, and KOH or TMAH anisotropic etching was a crucial step that decided the cross-sectional shape of the SiNWs. We obtained smooth, triangular SiNW structures with Si (111) sidewalls at an angle of 54.74° with (100) top and bottom surfaces (figure 9, inset). The fabricated SiNWs with single crystalline structure had large surface-to-volume ratio, and the triangular shape was beneficial for obtaining narrow SiNWs. Owing to the planarization of the anisotropic wet etching, the surface of SiNWs was fairly smooth. The width of the SiNW in the lateral direction was linearly proportional to the etching time with the lateral etching rate of approximately 2.3 nm min$^{-1}$ (50°C, 25% TMAH). Hence, the width of SiNW could be precisely controlled by varying the etching time. By finely controlling the etching time and thermal oxidation, we could decrease the diameter of nanowires down to 20 nm, as visualized in an SEM image (figure 9).

Figure 7. Close-up of a nanobeam in (110) SOI wafer.

Figure 8. Fabrication process of a nanowire by MEMS technology. (Online version in colour.)

We also developed a unique, precise size control approach and fabricated SCS nanostructure with high uniformity and simple procedures on a (111) silicon wafer. As shown in figure 10a–d,
Figure 9. Nanowire with a width and thickness of 20 nm.

Figure 10. The overall fabrication of SiNW by standard MEMS processes. (a) Oxidizing the (111) wafer; (b) mask windows patterning and BOE; (c) ion beam etching to a depth of \( t \); (d) KOH wet etching; (e) self-limiting oxidation; (f) BOE and supercritical-point drying.

The (111) wafer was first oxidized to a 350 nm thick SiO\(_2\) layer to function as etch mask for the following KOH wet etching process. Then, the SiO\(_2\) layer was patterned using standard photolithography process. Two tilted rectangular windows were formed side by side on the surface. SiO\(_2\) in etching windows was removed with buffered oxide etch (BOE), and Si underneath was dry etched approximately 1 \( \mu m \) deep by ion beam etching. After the lithography resist was cleaned, the wafer was etched in KOH (40%, 50\( ^\circ \)C) for 30 min. A \( \langle 110 \rangle \) -oriented silicon line was formed in between the two etching windows. The width of the silicon line was approximately 350 nm, of submicrometre scale.

Figure 11a is the top view of the etch cavity shape for the two tilted rectangle mask windows, whose two sides are along the two \( \langle 110 \rangle \) directions. After KOH wet etching, the rectangular windows became hexagon shaped. Therefore, the two rectangular cavities were etched to be two hexagon-shaped cavities with a silicon line formed in between. The silicon line is along \( \langle 110 \rangle \) direction, and its cross section is a parallelogram with an obliquity of 70.5\( ^\circ \). The length and width of the silicon line are determined by the dimensions and positions of the mask windows,
and the height by the etching depth $t$ shown in figure 10c. This method enables us to fabricate submicrometre-scaled silicon lines easily by standard MEMS processes. In this case, we set the lengths of the tilted rectangular window as 4 and 7 μm, respectively, and we could get a silicon line with the length of 4 μm and width of $\Delta x$, which can vary from 0 to any value, which is 1 μm in this experiment. The fabricated silicon line is shown in figure 11b. It is very straight and has a good dimensional uniformity, with length of approximately 4.2 μm and width of approximately 350 nm, not quite the designed values.

Further experiments indicate that the width of the wall structure can be preset precisely by using a wafer rotation angle during the wet etching mask window patterning. A resolution of 80 – 200 nm was achieved when the angle changed every 0.5°. We reduced the width of SCS wall from approximately 1.5 μm to 100 nm, and fabricated a suspended SiNW of 30 nm in width from the wall structure by self-limiting oxidation.

3. Nanoeffects with mechanical behaviour

Mechanical property measurements of nanostructures, such as nanobeams and nanowires, are very challenging because of the difficulties in (i) sample preparation and nanomanipulating and (ii) measuring force and displacement (strain and stress) with nanoscale resolution. But in recent years, researchers have demonstrated some mechanical tests on SCS nanobeams and nanowires, which cover bending tests, resonance tests and tensile tests.

(1) Bending tests: AFM is usually employed to give three-dimensional images of the topography of the sample surface, control and apply a specified amount of force on the
sample. It is suitable to use AFM in mechanical tests on a single- (double-) clamped nanobeam (nanowire) by applying force to the specimen and measure deformation simultaneously. By using beam bending equations, the mechanical properties can be deduced.

(2) Resonance tests: according to Euler–Bernoulli theory, dynamic studies on the resonant frequency of nanobeams and nanowires can provide Young’s modulus when the geometry is determined accurately.

(3) Tensile tests: to facilitate tensile testing on nanostructures, various nanomanipulators, based on multi-axes actuation, were designed to work with SEM or transmission electron microscopy (TEM). With nanostructure being stretched and tensile force being measured by nanomanipulators, sample elongation being observed by SEM or TEM, in situ tensile tests are carried out inside SEM and TEM instruments.

Among all the methods, tensile testing is more challenging because the specimens must be free-standing, clamped at both ends, stretched uniaxially and their elongation measured with nanometre resolution. MEMS can be advantageously employed in the testing of nanoscale samples. It usually consists of three parts: actuator for nanomanipulating sample, sensor for measuring force on the sample and a cofabricated (or later-attached) sample. By integrating MEMS chip with SEM or TEM, we have successfully performed several tensile tests on nanostructures.

(a) Micro-electro-mechanical systems tensile-testing chip for in situ observation in scanning electron microscope and transmission electron microscope [36,37]

It is very difficult to perform a tensile test on SCS nanostructures because of two main difficulties: (i) sample preparation and nanomanipulating and (ii) measuring force and displacement (strain and stress) at nanoscale. A promising solution is the MEMS-based tensile test in SEM and TEM.

A suspended SCS nanobeam, a comb drive actuator, a force sensor beam and an electron beam window were integrated into the chip, as schematically shown in figure 12. The three supporting beams ensured the stretching force to be uniaxial. When the in situ tensile test was carried out, the comb drive actuator pulled the movable structures, the SCS nanobeam would be stretched and the force sensor beam would be bent. Both the deformation of the nanobeam and the deflection of the force sensor beam could be measured through TEM.

The comb drive actuator makes use of tangential electrostatic force of pairs of parallel plates for driving. This force pulls the movable combs to more overlapping area with the fixed combs. The higher the voltage applied, the larger the pulling force will be. But the forces calculated from equation (3.1) at different actuating voltages might quite differ from the real values owing to dimensional non-uniformity of the combs after the chip fabricating process. Therefore, a force
sensor beam was designed to measure the tensile force. To suit the 0.9 mm pole piece gap in a JOEL 2010, the sample-containing region in our custom-made TEM holder required the MEMS tensile-testing chip to be 9 $\times$ 5 $\times$ 0.5 mm. The chip was fabricated by bonding an SOI wafer and a silicon wafer together. The SCS nanobeam, combs and microbeams were made on the SOI wafer side and the electron beam window on the silicon wafer side.

The process is illustrated in figure 13, where the side views are on the left and cross-sectional views on the right. A (100) SOI wafer, with a 200 nm top SCS layer and a 375 nm buried oxide layer, was dry oxidized to reduce the thickness of the top Si layer to 90 nm. The non-uniformity of the SCS layer was mainly caused by the non-uniform interface between the SCS layer and the buried oxide layer and was of 5 nm. The wafer was patterned and 10 $\mu$m deep trenches were dry etched to be used as gaps for the movable structures, which were made on the backside. The ⟨110⟩-oriented nanobeam was also shaped at this step. Another wafer, with a thickness of 400 $\mu$m, was oxidized to a 2 $\mu$m SiO$_2$ layer, then a through hole was made on it by DRIE (deep reactive ion etch) to serve as the electron beam window. These two wafers were aligned with each other in KarlSuss MA6 and pre-bonded in SB6. The bonding conditions were set as 500°C and 2 bar pressure for 15 min. Afterwards, the pre-bonded wafers were annealed at 1000°C for 1 h. Then, the bonded wafers were ground and polished on the SOI wafer’s backside to reduce the thickness of its back Si layer to 100 $\mu$m. A 1 $\mu$m thick Al layer was deposited on this new surface and the Al pads were patterned. Still on this surface, all structures, including combs and microbeams, were patterned and processed by DRIE. Finally, the SiO$_2$ layers around SCS nanobeam were removed by BOE. The structures were released by CO$_2$ supercritical drying.

Figure 14 gives the SEM view of the MEMS chip, with a sample (SCS nanobeam), a comb drive actuator, a force sensor beam and a TEM electron beam window being integrated into it, and those parts are fabricated in one process. As the electrostatic force-actuated comb drive actuator causes no current, it causes no interference to TEM measurements.
(b) Young’s modulus size effect of silicon nanobeam [44]

With the developed process, four MEMS tensile testing chips integrated with ⟨110⟩-oriented SCS nanobeams were achieved in an SOI wafer with thickness from 45 to 100 nm. Mounting the chips onto a custom-made TEM sample holder, in situ TEM tensile tests were carried out to study Young’s modulus at different nanobeam thicknesses.

When actuating voltage was applied, with the on-chip comb drive actuator stretching the SCS nanobeam and in situ TEM observation, tensile tests were performed on the sample. For actuating voltages from 50 to 100 V, incremented in 10 V steps, we snapshot the movements of the two ends of the nanobeam, A and B (indicated by the arrows), as shown in figure 15. By taking the four corner marks, which were the images of four fixing film clamps in TEM, as reference positions, we measured the displacements of A and B. The elongation of the nanobeam can be obtained from the difference and the deflection of the force sensor beam can be considered as the displacements of A. The tensile force on the SCS nanobeam was calculated, with the elastic constant of the force sensor beam. By fitting the strain–stress relationship under different actuating voltages, we obtained the Young’s modulus.

The relationship of Young’s modulus (E) and the nanobeam thickness (h) is presented in figure 16; also presented in the figure are results of resonance tests [30], pull-in tests [65] and our work [41] of tensile tests in SEM. It can be seen that the measured Young’s modulus (from 74 to 178 GPa) is well in agreement with our previous results of tensile tests in SEM. The measured E decreased monotonically with the decreasing thickness of the SCS nanobeams, which qualitatively matches the relations obtained by resonant tests and pull-in tests. But in resonant/pull-in tests, Young’s modulus showed the decreasing tendency earlier compared with the tensile tests. These three sets of Young’s moduli appear to approach one value when the nanobeam’s thickness approaches approximately 40 nm, and this Young’s modulus value is very close to Young’s modulus of silicon dioxide.

(c) Determination of the lattice parameters of silicon nanobeam [49]

During uniaxial tensile testing, we can also observe the lattice behaviour of an SCS nanobeam. To avoid the challenge of integration of nanomanipulation and preparation of nanomaterial, we developed a unique specimen fabrication process that can be used to prepare MEMS testing device and SCS nanobelt simultaneously. Lattice parameters measured by selected-area electron diffraction (SAED) are obtained during the tensile test.
Figure 15. TEM bright field image of the structures and the SAED pattern of the SCS nanobeam (inset). TEM images of the movements of the two ends of the nanobeam, A and B (indicated by arrows).

Figure 16. Young’s modulus—thickness relationship for the SCS nanobeam by TEM tensile tests (triangles); also shown in the figure are results of SEM tensile tests (inverted triangles) [41], resonance tests (circles) [30] and pull-in tests (squares) [65]. (Online version in colour.)

As the electron beam went through the SCS nanobeam, it would be diffracted by the lattice and SAED pattern would form on the TEM imaging plane. Figure 17 demonstrates both two-dimensional lattice parameters and SAED pattern of (100) SCS.

The relationship between the lattice parameters and dimensional parameters of SAED pattern can be deduced from the basic theory of electron diffraction and given as

\[
\begin{align*}
\alpha &= \cos^{-1}\left(\frac{j^2 - j^2 - 2ij \cos \varphi}{i^2 + j^2 + 2ij \cos \varphi}\right), \\
a &= \frac{4L \lambda}{i}, \\
b &= \frac{4L \lambda}{j},
\end{align*}
\]

(3.1)
Figure 17. Basic parameters of SAED of (100) silicon. (a) Two-dimensional lattice parameters of (100) silicon, (b) SAED pattern of (100) silicon. (Online version in colour.)

Figure 18. (a–c) Lattice parameters of the SCS nanobeam with different actuating voltages. (d) A ⟨110⟩-oriented stretched lattice model of SCS nanobelt. (Online version in colour.)

where $a$, $b$, $\alpha$ and $i$, $j$, $\varphi$ are presented in figure 17a,b, respectively, $L$ is the camera length of TEM and $\lambda$ is the wavelength of the accelerated electron.

Usually more than three diffraction spots can be obtained from a single SAED pattern (figure 17b), hence equation (3.1) becomes overdetermined. Therefore, to use all diffraction spots adequately and to reduce the uncertainty of the calculated results, the least-squares method is used in the data processing. In one word, the lattice parameters of silicon nanobeam can be calculated from the SAED pattern of (100) silicon using equation (3.1).

The results are presented in figure 18. The voltage of the comb drive actuator is used for representing different levels of tensile force. By statistically calculating the lattice parameters from more than 10 patterns of each driving voltage and using the least-squares fitting method to adequately use all diffraction spots in each pattern, it was possible to reduce the statistical
measurement error to approximately 0.003 nm. Figure 18a–c shows that the lattice parameters $a$ and $b$ basically maintain a constant value, 0.553 nm. This result can be explained by the [110]-oriented stretched lattice model (figure 18d). As shown in figure 18d, under the condition of small strain, under [110]-oriented tensile stress the [110] interplanar spacing would increase, while the [110] interplanar distance perpendicular to tensile stress would decrease owing to the least-energy principle. The principle, in which the atomic bond which links two silicon atoms tends to remain constant, leads to the lattice parameters $a$ and $b$ being unchanged under a small stress and is also the fundamental mechanism of Poisson’s ratio of a material.

These results suggest that the trends of lattice parameters are in agreement with the increasing tensile stress model of the SCS nanobelt. Furthermore, the fact that the local strain calculated from the ⟨110⟩ stretched lattice model is consistent with the average strain of the nanobelt confirms the stress distribution uniformity of the SCS nanobelt.

4. Nanodevices and sensors based on field-effect transistors

One-dimensional nanostructures have proved to be promising candidates for recognizing a wide range of biological and chemical species. Semiconducting nanowire field-effect transistors (FETs) [66,67], one of the most promising platforms for unlabelled sensing, are emerging as powerful sensors for recognizing a wide range of biological and chemical species [68] with many attractive properties including low cost, ultrahigh sensitivity, direct electrical readout and multiplexed detection [69,70]. SiNW-based FETs have been exhibited. The sensing mechanism for an SiNW biosensor operated as an FET is charged-molecule-induced field effect on the carrier conduction inside the nanowires [71,72]. The enhanced sensitivity of nanodevices, capable of sensing the presence of even a small quantity of charged species by their intrinsic charge, is mainly owing to their comparable size with molecules and large surface: volume ratio [73]. By exploiting this attractive property, a variety of SiNW–FET nanosensor devices have been designed for the detection of various targets including DNA [34], proteins [66–68], small molecules [69], metal ions and chemical species [67,70,71], single virus particles [72] and even cells [73].

(a) Piezoresistive sensing in an Si nanobeam [50]

A novel piezoresistive sensing scheme for nanostructures has been presented, as illustrated in figure 19. A metal–oxide–semiconductor (MOS) capacitor is fabricated on a boron-doped nanobeam. During working, the gate voltage is biased to be larger than the threshold voltage, while the substrate beneath the depletion layer of the MOS capacitor is used as piezoresistor. As the maximum width of the depletion layer is determined by the doping level and does not change with the bias voltage, the piezoresistor beneath the MOS capacitor is expected to be voltage independent. The maximum depletion layer width should be larger than the half thickness of the beam to avoid cancellation of piezoresistive effects beside the neutral plane. As the piezoresistor is on the bottom surface of the nanobeam, high sensitivity may be achieved.

The process flow of a double-clamped beam with piezoresistor beneath the MOS capacitor is shown in figure 20. The thickness of top silicon is reduced to 160 nm by thermal oxidation of a SOI wafer. A heavy dose of boron is applied to the beam region to reduce its resistance, as shown in

![Figure 19. Piezoresistor beneath the MOS capacitor.](image-url)
Figure 20. (a–e) Process flow of piezoresistor beneath the MOS capacitor.

Figure 21. SEM image of the nanobeam with the sensing piezoresistor.

Figure 22. The measured resistance responses versus the gate voltage. Squares denote measurement and solid line denotes theory. (Online version in colour.)

A light dose of boron is applied on the gate region with an energy of 25 keV and dose of $4 \times 10^{12}$ cm$^{-2}$, as shown in figure 20b. Beam structure is patterned by DRIE. The length and width of the beam are 46 and 7 $\mu$m, respectively. An oxide layer of 30 nm is thermally grown to serve as the gate oxide. The gate is formed by 50 nm TiW and 100 nm Au, as shown in figure 20c. A layer of 700 nm of amorphous Si is deposited by plasma-enhanced chemical vapour deposition and holes for electrical connection are formed by dry etch. Metal wires are electroplated and amorphous Si is removed by RIE, as shown in figure 20d. CF4 and BHF are used to release the beam, as shown in figure 20e.
The fabricated nanobeam structure is shown in figure 21. The slight bending of the nanobeam is owing to the residual stress after the fabrication process. The beam thickness is measured to be 149 nm. The resistance response with the gate voltage is measured using a semiconductor parameter analyzer (Agilent 4156) and plotted in figure 22. The resistance rises with increasing gate voltage and almost remains constant for gate voltage larger than 4 V, which corresponds to the threshold voltage. The measured resistance of the piezoresistor is 28.2 kΩ after the strong inversion. The piezoresistor beneath the MOS capacitor is used to measure the amplitude–frequency response of the nanobeam at atmospheric pressure, as shown in figure 23. The measured resonant frequency is 3.973 MHz, which matches the optical measurement (3.998 MHz) by laser Doppler vibrometry (Polytec MSA-500).
Figure 25. Uniformity of the fabricated SiNWs. (a) Distribution of the width of a batch of SiNWs is shown in columns. The anticipative width of the SiNWs is 60 nm and 14 SiNWs are counted in total. (b) Column plot of the conductance of different fabricated SiNWs. Twelve SiNWs were measured in total. The length and width of the SiNWs were 6 μm and 100 nm, respectively. P-type and boron-doped nanowires were used in these experiments.

(b) Silicon nanowire–field-effect transistor [45]

A prototype FET device was fabricated with the SiNW array (figure 24a). The SiNW–FET devices demonstrated excellent electrical properties, as shown in figure 24b,c. Particularly, we observed almost no electronic hysteresis, suggesting the presence of a low density of trapped charges inside the structure. However, it is interesting that our SiNW–FETs rapidly and sensitively responded to the pH change of the solution when SiNWs were silanized at the exposed, dominant Si(111) planes, which is preferred for selective surface functionalization, suggesting that this device is particularly appropriate for sensing.

Moreover, the fabricated nanowires also have well-distributed sizes and uniform conductance in statistics (figure 25). The fabricated arrays contain 16 uniform and well-aligned SiNWs of both p-type and n-type. The incorporation of both p-type and n-type nanowires in a single chip allows...
effective discrimination of possible electrical cross-talk and false-positive signals by correlating the response versus time from the two types of device elements. Optical microscopic observation confirmed that the aligned SiNWs were uniform and well ordered. These studies showed that the CMOS-compatible sensor array could be conveniently fabricated with high controllability, reproducibility and throughput.

(c) Super-sensitive biosensor based on silicon nanowires [45,47]

We employed the n-type SiNW–FET device to electrically detect DNA hybridization. Capture probe DNA with a terminal carboxyl group was conjugated to the amine of (3-aminopropyl)triethoxysilane (APTES)-modified SiNWs, with the help of N-hydroxysuccinimide and 1-ethyl-3-(3-dimethylaminopropyl)carbodiimide (figure 26). When the buffer solution was flowed through the sensor surface, the electrical response of the SiNW–FET remained nearly unchanged. Significantly, when a solution containing 1 nM of fully complementary target DNA was introduced, we observed a rapid decrease in the electrical current down to nearly half of the initial value within seconds. Of note, the hybridization process could be monitored in real time with this SiNW–FET sensor. The decrease in electrical current suggested that the binding of negatively charged target DNA to the gate dielectric of n-type SiNW–FET results in the depletion of carriers. As a control experiment, target DNA of the same concentration was flowed through an
unmodified SiNW–FET, which did not lead to significant current change, suggesting the absence of non-specific binding of target DNA to the SiNW surface.

Further experiment indicates that this SiNW–FET nanosensor revealed ultrahigh sensitivity for rapid and reliable detection of 1 fM of target DNA and high specificity single-nucleotide polymorphism discrimination. As a proof-of-concept for multiplex detection with this small size and mass-producible sensor array, we demonstrated simultaneous selective detection of two pathogenic strain virus DNA sequences (H1N1 and H5N1) of avian influenza.

As the sensing mechanism of SiNW–FET can be understood in terms of the change in charge density at the SiNW surface after hybridization, there have been limited systematic studies on fundamental factors related to device sensitivity to further make clear the overall effect on sensing sensitivity. Here, we present an analytical result for our triangular cross-sectional wire for predicting the sensitivity of nanowire surface-charge sensors as shown in figure 27. It was confirmed through sensing experiments that the back-gated SiNW–FET sensor had the highest percentage current response in the subthreshold regime and the sensor performance could be optimized in low buffer ionic strength and at moderate probe concentration. The optimized SiNW–FET nanosensor revealed ultrahigh sensitivity for rapid and reliable detection of target DNA with a detection limit of 0.1 fM and high specificity for single-nucleotide polymorphism discrimination. In our work, enhanced sensing of biological species by optimization of operating parameters and fundamental understanding for SiNW–FET detection limit was obtained.

5. Summary

With our nanofabrication method based on MEMS technology, we have proved that smart design and carefully controlled processes are the key points in these nanoapplications. It can mean nanostructures and even nanodevices can be integrated conveniently with microstructures, which promises low cost and batch productivity and, simultaneously, may accelerate the application of nanodevices in the future.

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